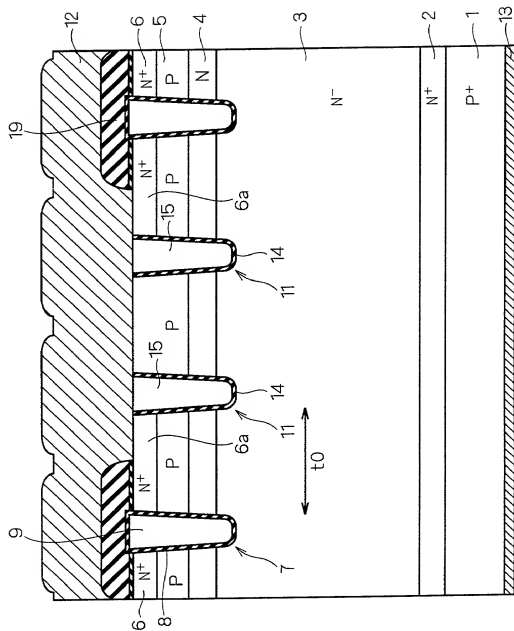


[illegible]

FIG. 5



The figure consists of two cross-sectional views of a layered material structure. The top view shows a central core layer labeled 11, which is flanked by two side layers labeled 14. The bottom view shows a more complex structure with multiple layers. On the left side, there are layers labeled 6b, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, and 19. On the right side, there are layers labeled 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, and 19. The central core layer 11 is shown as a dashed line. The layers are separated by interfaces, some of which are indicated by arrows and labels A and B.

FIG. 7

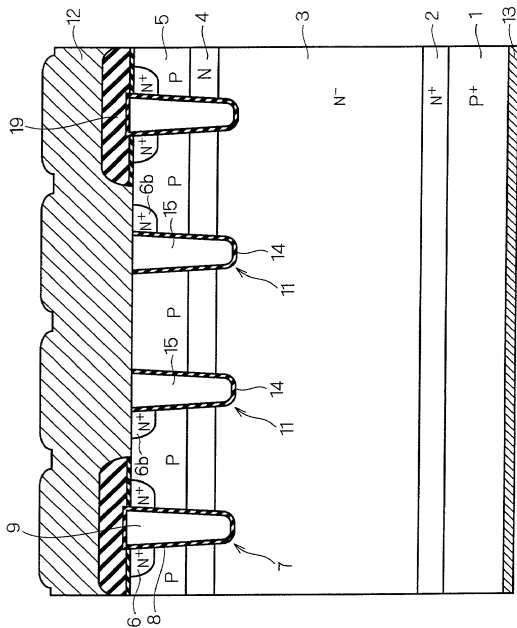


FIG. 8

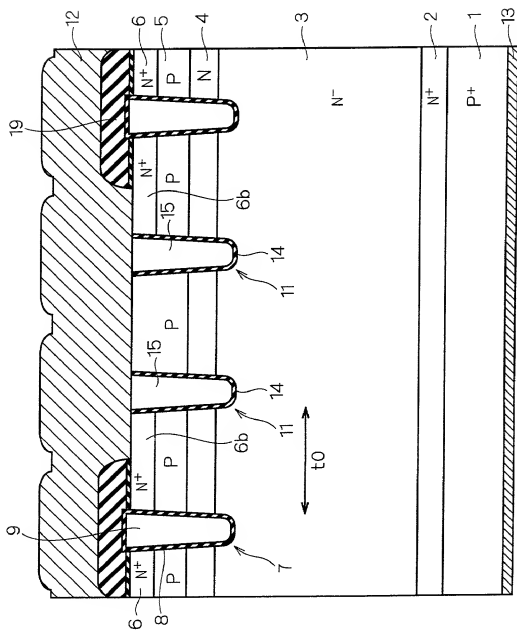


FIG. 9

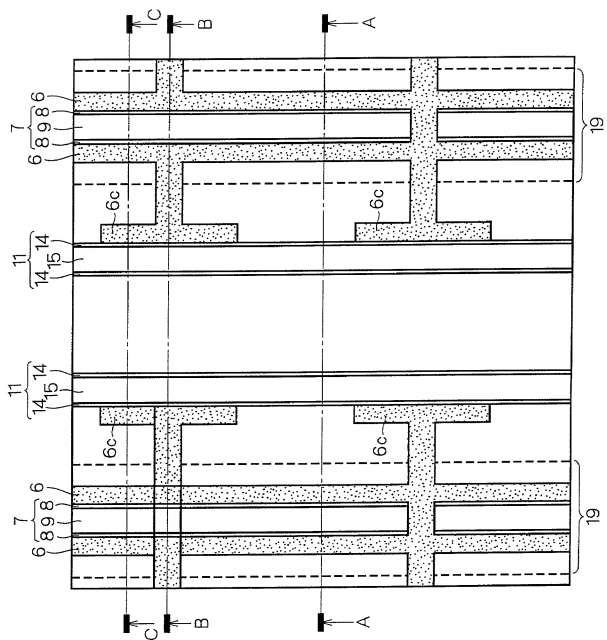
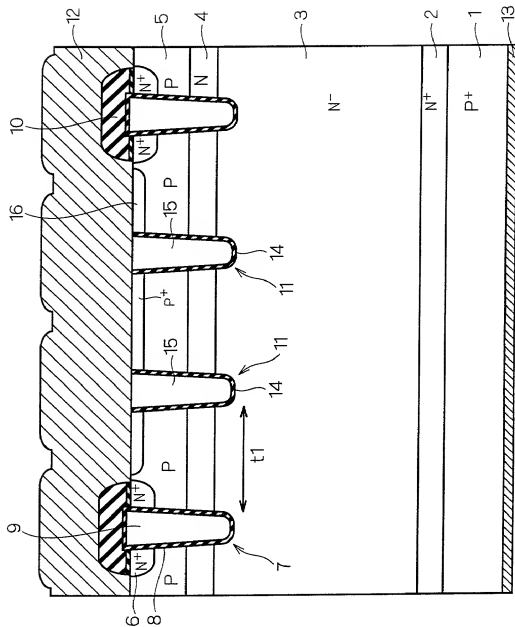


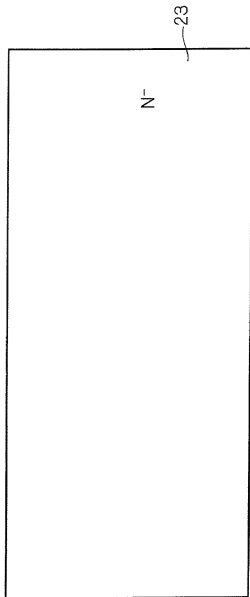
FIG. 10



[illegible]

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FIG. 12



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FIG. 14

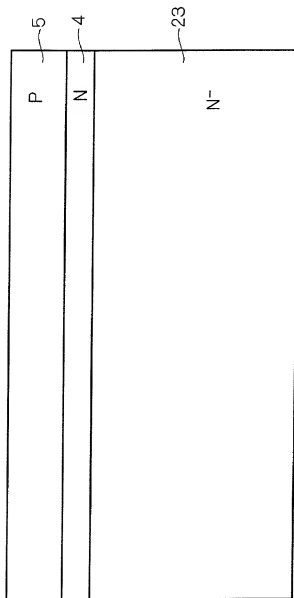


FIG. 15

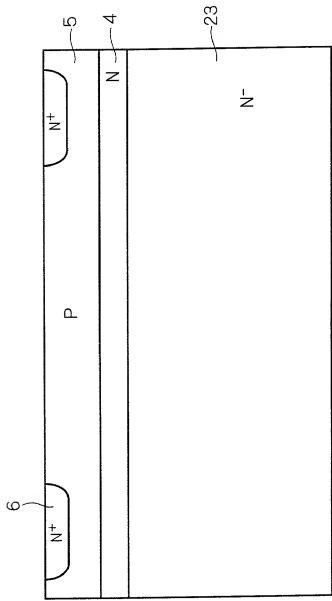


FIG. 16

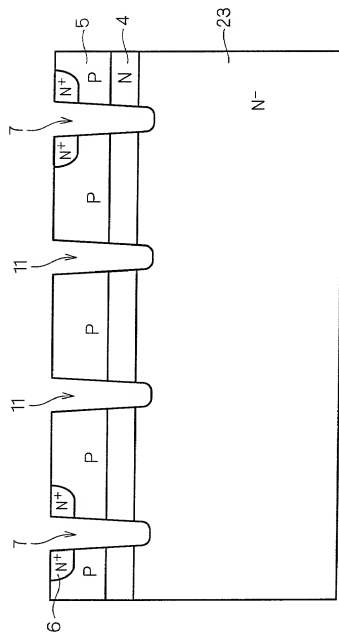


FIG. 17

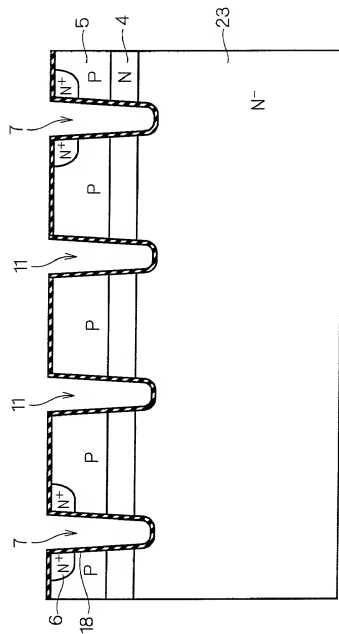


FIG. 18

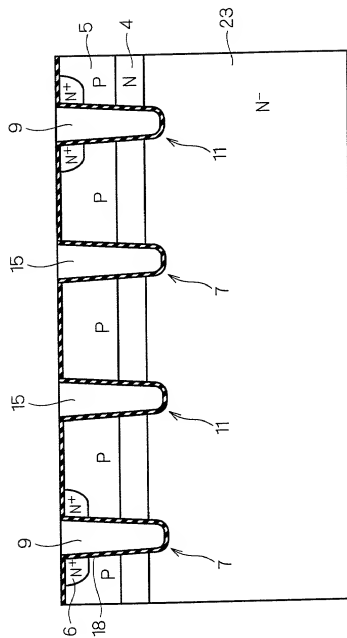


FIG. 19

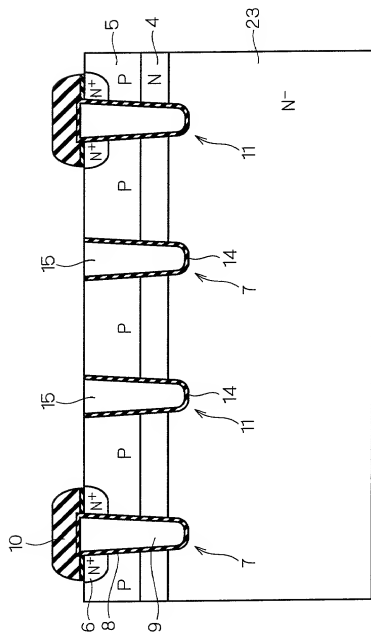


FIG. 20

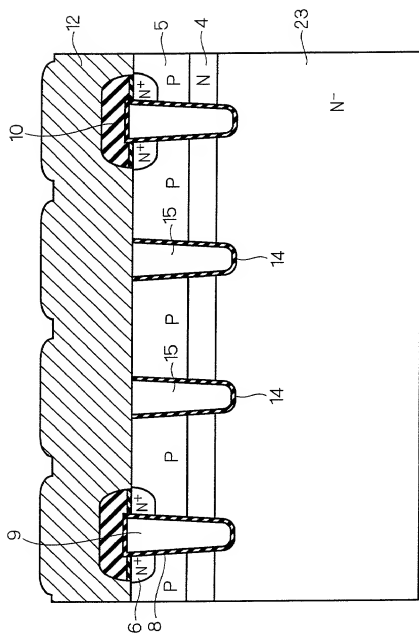


FIG. 21

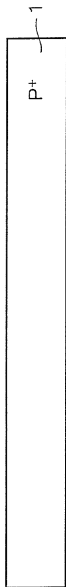


FIG. 22

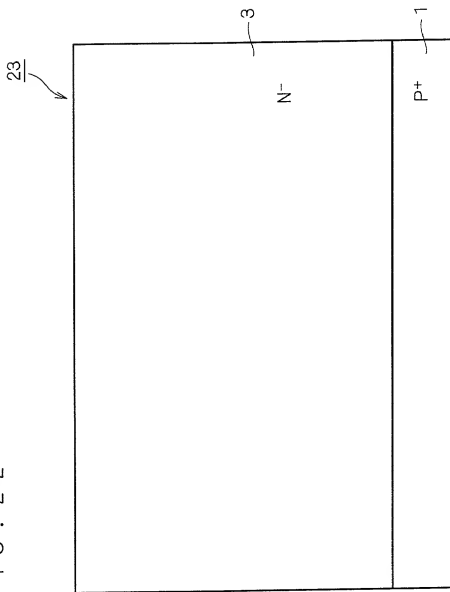
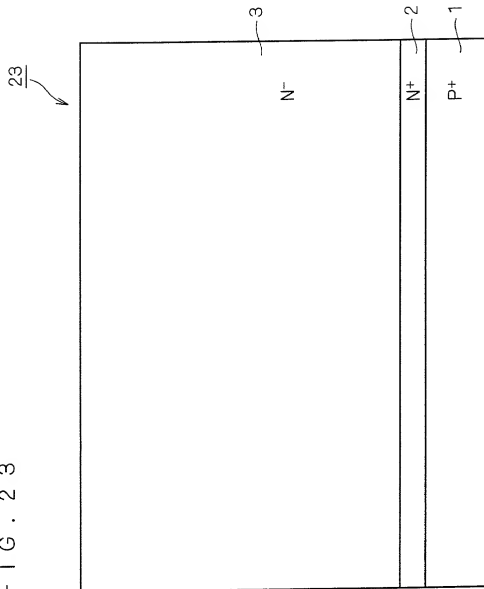


FIG. 23



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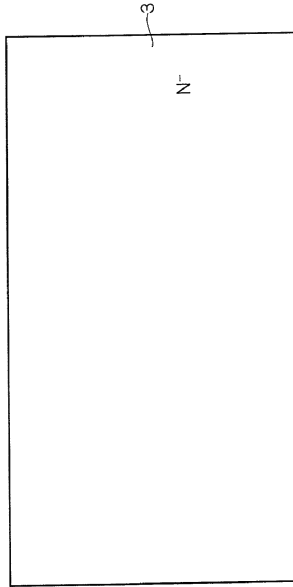


FIG. 24

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FIG. 25

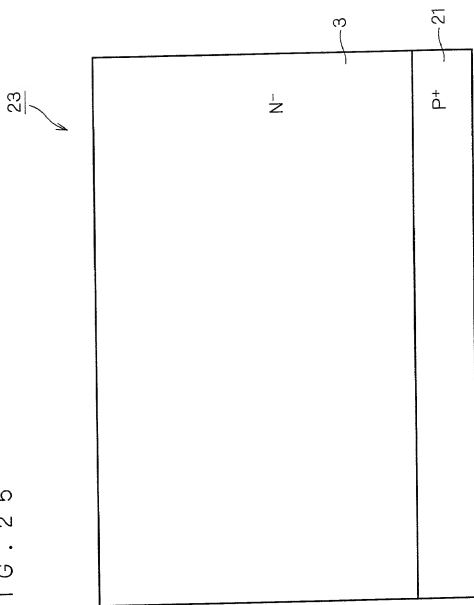


FIG. 26

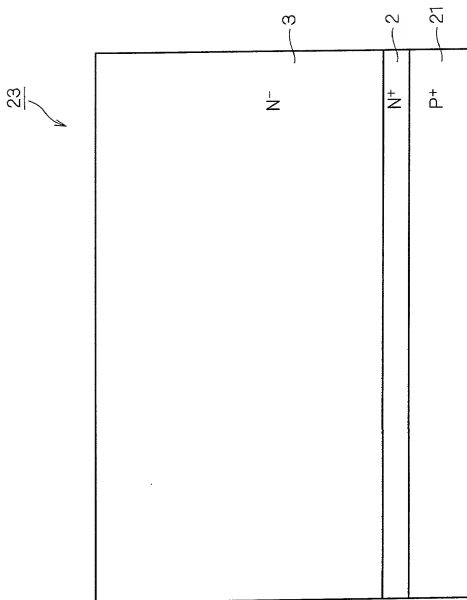
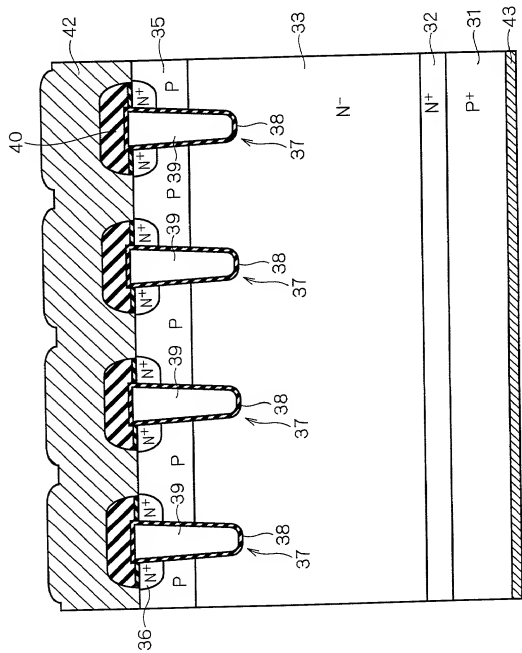


FIG. 26

FIG. 27



This cross-sectional view shows a semiconductor device with a substrate 36. The substrate has a top layer 31 (P+) and a bottom layer 32 (N+). Four vertical structures are formed on the substrate. Each structure consists of a base 37 and a top cap 38. The base 37 is made of N+ material and is surrounded by a P region 39. The top cap 38 is made of N+ material. The structures are separated by a dielectric material 40. The top surface of the device is a P layer 34, and the bottom surface is an N layer 35. A layer 42 is also shown on the top surface.

FIG. 29

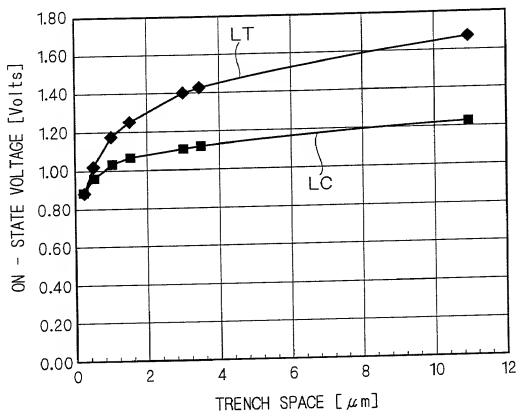
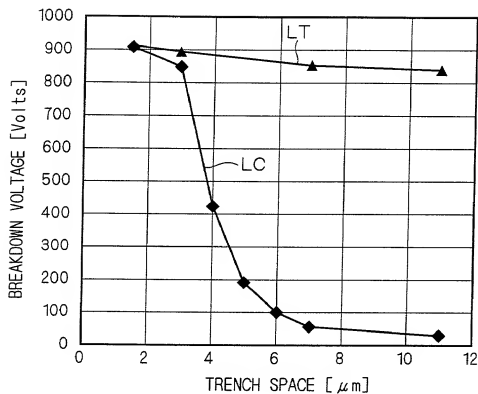


FIG. 30



[illegible]

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SHEET 32 OF 32